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IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

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1. **Testing embedded-core-based system chips**
Zorian, Y.; Marinissen, E.J.; Dey, S.;
Computer
Volume 32, Issue 6, June 1999 Page(s):52 - 60
Digital Object Identifier 10.1109/2.769444
AbstractPlus | References | Full Text: PDF(204 KB) IEEE JNL
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2. **Testing embedded-core based system chips**
Zorian, Y.; Marinissen, E.J.; Dey, S.;
Test Conference, 1998. Proceedings. International
18-23 Oct. 1998 Page(s):130 - 143
Digital Object Identifier 10.1109/TEST.1998.743146
AbstractPlus | Full Text: PDF(1340 KB) IEEE CNF
Rights and Permissions

3. **Introducing core-based system design**
Gupta, R.K.; Zorian, Y.;
Design & Test of Computers, IEEE
Volume 14, Issue 4, Oct.-Dec. 1997 Page(s):15 - 25
Digital Object Identifier 10.1109/54.632877
AbstractPlus | References | Full Text: PDF(228 KB) IEEE JNL
Rights and Permissions

4. **VHDL modeling and model testing for DSP applications**
Armstrong, J.R.; Gray, F.G.; Meng-Wei Lin;
Industrial Electronics, IEEE Transactions on
Volume 46, Issue 1, Feb. 1999 Page(s):13 - 22
Digital Object Identifier 10.1109/41.744371
AbstractPlus | References | Full Text: PDF(592 KB) IEEE JNL
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Results for "(isolation logic and power and design<in>metadata) and simulat*"

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» Key

IEEE JNL	IEEE Journal or Magazine
IET JNL	IET Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

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1. **Automatic ADL-based Operand Isolation for Embedded Processors**
Chattopadhyay, A.; Geukes, B.; Kammler, D.; Witte, E.M.; Schliebusch, O.; Ishebabi, H.; Leupers, I H.;
Design, Automation and Test in Europe, 2006. DATE '06. Proceedings
Volume 1, 6-10 March 2006 Page(s):1 - 6
AbstractPlus | Full Text: PDF(160 KB) IEEE CNF
Rights and Permissions

2. **System-on-chip testability using LSSD scan structures**
Zarrineh, K.; Upadhyaya, S.J.; Chickermane, V.;
Design & Test of Computers, IEEE
Volume 18, Issue 3, May-June 2001 Page(s):83 - 97
Digital Object Identifier 10.1109/54.922805
AbstractPlus | References | Full Text: PDF(156 KB) IEEE JNL
Rights and Permissions

3. **A sequential failure detection technique and its application**
Tze-Thong Chen; Adams, M.;
Automatic Control, IEEE Transactions on
Volume 21, Issue 5, Oct 1976 Page(s):750 - 757
AbstractPlus | Full Text: PDF(752 KB) IEEE JNL
Rights and Permissions

4. **Integrating development- and support tools for PHM in Saab 39 Gripen**
Fransson, T.;
Aerospace Conference, 2006 IEEE
4-11 March 2006 Page(s):12 pp.
Digital Object Identifier 10.1109/AERO.2006.1656071
AbstractPlus | Full Text: PDF(1248 KB) IEEE CNF
Rights and Permissions

5. **Nonlinear Fault Detection and Isolation in a Three-Tank Heating System**
Mattone, R.; De Luca, A.;
Control Systems Technology, IEEE Transactions on
Volume 14, Issue 6, Nov. 2006 Page(s):1158 - 1166
Digital Object Identifier 10.1109/TCST.2006.880221
AbstractPlus | Full Text: PDF(480 KB) IEEE JNL

Terms used
simulat and **test pattern?** and **path?** and **library** and **reuse**

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Relevance scale

1 Fast detection of communication patterns in distributed executions

Thomas Kunz, Michiel F. H. Seuren

November 1997 **Proceedings of the 1997 conference of the Centre for Advanced Studies on Collaborative research CASCON '97**

Publisher: IBM Press

Full text available: pdf(4.21 MB) Additional Information: full citation, abstract, references, index terms

Understanding distributed applications is a tedious and difficult task. Visualizations based on process-time diagrams are often used to obtain a better understanding of the execution of the application. The visualization tool we use is Poet, an event tracer developed at the University of Waterloo. However, these diagrams are often very complex and do not provide the user with the desired overview of the application. In our experience, such tools display repeated occurrences of non-trivial commun ...

2 Frontmatter (TOC, Letters, Philosophy of computer science, Interviewers needed, Taking software requirements creation from folklore to analysis, SW components and product lines: from business to systems and technology, Software engineering survey)

September 2005 **ACM SIGSOFT Software Engineering Notes**, Volume 30 Issue 5

Publisher: ACM Press

Full text available: pdf(1.98 MB) Additional Information: full citation, index terms

3 IP Design and Reuse: Application of Software design patterns to DSP library design

Pontus Åström, Stefan Johansson, Peter Nilsson

September 2001 **Proceedings of the 14th international symposium on Systems synthesis ISSS '01**

Publisher: ACM Press

Full text available: pdf(144.85 KB) Additional Information: full citation, abstract, references, citings, index terms

The design of a hardware data path library is one of the harder problems in design for reuse. Thanks to the appearance of hardware modeling libraries based on C++, it is possible to apply advanced software techniques to design such a library. This paper shows how software design patterns can be applied to hardware design. Design patterns yield a twofold advantage: a faster design process, and a library that is more extensible and

modular than an equivalent HDL counterpart. From a VHDL-C++ design ...

4 GPGPU: general purpose computation on graphics hardware

David Luebke, Mark Harris, Jens Krüger, Tim Purcell, Naga Govindaraju, Ian Buck, Cliff Woolley, Aaron Lefohn

August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

Publisher: ACM Press

Full text available: pdf(63.03 MB) Additional Information: full citation, abstract, citings

The graphics processor (GPU) on today's commodity video cards has evolved into an extremely powerful and flexible processor. The latest graphics architectures provide tremendous memory bandwidth and computational horsepower, with fully programmable vertex and pixel processing units that support vector operations up to full IEEE floating point precision. High level languages have emerged for graphics hardware, making this computational power accessible. Architecturally, GPUs are highly parallel s ...

5 Delay test and BIST: TranGen: a SAT-based ATPG for path-oriented transition faults

Kai Yang, Kwang-Ting Cheng, Li-C. Wang

January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04 , Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04**

Publisher: IEEE Press

Full text available: pdf(118.88 KB) Publisher Site Additional Information: full citation, abstract, references, citings

This paper presents a SAT-based ATPG tool targeting on a path-oriented transition fault model. Under this fault model, a transition fault is detected through the longest sensitizable path. In the ATPG process, we utilize an efficient false-path pruning technique to identify the longest sensitizable path through each fault site. We demonstrate that our new SAT-based ATPG can be orders-of-magnitude faster than a commercial ATPG tool. To demonstrate the quality of the tests generated by our approac ...

6 The elements of nature: interactive and realistic techniques

Oliver Deusen, David S. Ebert, Ron Fedkiw, F. Kenton Musgrave, Przemyslaw Prusinkiewicz, Doug Roble, Jos Stam, Jerry Tessendorf

August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

Publisher: ACM Press

Full text available: pdf(17.65 MB) Additional Information: full citation, abstract

This updated course on simulating natural phenomena will cover the latest research and production techniques for simulating most of the elements of nature. The presenters will provide movie production, interactive simulation, and research perspectives on the difficult task of photorealistic modeling, rendering, and animation of natural phenomena. The course offers a nice balance of the latest interactive graphics hardware-based simulation techniques and the latest physics-based simulation techni ...

7 An RTL Methodology to Enable Low Overhead Combinational Testing

Subhrajit Bhattacharya, Sujit Dey, Bhaskar Sengupta

March 1997 **Proceedings of the 1997 European conference on Design and Test EDTC '97**

Publisher: IEEE Computer Society

Full text available: pdf(872.56 KB) Publisher Site Additional Information: full citation, abstract

This paper introduces a low overhead test methodology, RT-SCAN, applicable to RT Level

designs. The methodology enables using combinational test patterns for testing the circuit, as done by traditional full-scan or parallel-scan schemes. However, by exploiting existing connectivity of registers through multiplexors and functional units, RT-SCAN reduces area overhead and test application times significantly compared to full-scan and parallel-scan schemes. Unlike most of the existing high-level te ...

Keywords: combinational circuits, RTL methodology, combinational testing, functional unit, RT-SCAN, multiplexor, register connectivity, application time, ATPG tool, area overhead, high-level test synthesis

8 Level set and PDE methods for computer graphics

David Breen, Ron Fedkiw, Ken Museth, Stanley Osher, Guillermo Sapiro, Ross Whitaker

August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

Publisher: ACM Press

Full text available: pdf(17.07 MB) Additional Information: full citation, abstract, citings

Level set methods, an important class of partial differential equation (PDE) methods, define dynamic surfaces implicitly as the level set (iso-surface) of a sampled, evolving nD function. The course begins with preparatory material that introduces the concept of using partial differential equations to solve problems in computer graphics, geometric modeling and computer vision. This will include the structure and behavior of several different types of differential equations, e.g. the level set eq ...

9 A software engineering perspective on algorithmics

Karsten Weihe

March 2001 **ACM Computing Surveys (CSUR)**, Volume 33 Issue 1

Publisher: ACM Press

Full text available: pdf(1.62 MB) Additional Information: full citation, abstract, references, index terms, review

An algorithm component is an implementation of an algorithm which is not intended to be a stand-alone module, but to perform a specific task within a large software package or even within several distinct software packages. Therefore, the design of algorithm components must also incorporate software-engineering aspects. A key design goal is adaptability. This goal is important for maintenance throughout a project, prototypical development, and reuse in new, unforseen contex ...

Keywords: algorithm engineering

10 Computing curricula 2001

September 2001 **Journal on Educational Resources in Computing (JERIC)**

Publisher: ACM Press

Full text available: pdf(613.63 KB) html(2.78 KB) Additional Information: full citation, references, citings, index terms

11 Test (co-organized with LA-TTTC): Reducing test time with processor reuse in network-on-chip based systems

Alexandre M. Amory, Érika Cota, Marcelo Lubaszewski, Fernando G. Moraes

September 2004 **Proceedings of the 17th symposium on Integrated circuits and system design SBCCI '04**

Publisher: ACM Press

Full text available: pdf(192.49 KB) Additional Information: full citation, abstract, references, index terms

This paper proposes a test planning method capable of reusing available processors as test sources and sinks, and the on-chip network as the access mechanism for the test of cores embedded into a system on chip. The resulting test time of the system is evaluated considering the number of reused processors, the number of external interfaces, and power dissipation. Experimental results for a set of industrial examples based on the ITC'02 benchmarks show that the cooperative use of both the on-chip ...

Keywords: NoC testing, SoC test, computer-aided test (CAT), core-based test, network-on-chip, software-based test

12 Special issue: AI in engineering

D. Sriram, R. Joobbani
April 1985 **ACM SIGART Bulletin**, Issue 92
Publisher: ACM Press
Full text available: pdf(8.79 MB) Additional Information: full citation, abstract

The papers in this special issue were compiled from responses to the announcement in the July 1984 issue of the SIGART newsletter and notices posted over the ARPAnet. The interest being shown in this area is reflected in the sixty papers received from over six countries. About half the papers were received over the computer network.

13 Frontmatter (TOC, Letters, Election results, Software Reliability Resources!, Computing Curricula 2004 and the Software Engineering Volume SE2004, Software Reuse Research, ICSE 2005 Forward)

July 2005 **ACM SIGSOFT Software Engineering Notes**, Volume 30 Issue 4
Publisher: ACM Press
Full text available: pdf(6.19 MB) Additional Information: full citation, index terms

14 The multics system: an examination of its structure

Elliott I. Organick
January 1972 Book
Publisher: MIT Press
Full text available: pdf(23.94 MB) Additional Information: full citation, abstract, references, cited by, index terms

This volume provides an overview of the Multics system developed at M.I.T.--a time-shared, general purpose utility like system with third-generation software. The advantage that this new system has over its predecessors lies in its expanded capacity to manipulate and file information on several levels and to police and control access to data in its various files. On the invitation of M.I.T.'s Project MAC, Elliott Organick developed over a period of years an explanation of the workings; concep ...

15 VLSI Circuits: Selective-run built-in self-test using an embedded processor

Sungbae Hwang, Jacob A. Abraham
April 2002 **Proceedings of the 12th ACM Great Lakes symposium on VLSI GLSVLSI '02**
Publisher: ACM Press
Full text available: pdf(181.75 KB) Additional Information: full citation, abstract, references, citings, index terms

Many systems-on-a-chip (SOCs) include processors as central units to implement diverse algorithms and control peripheral units such as embedded cores. The computing power of the embedded processor can be used to self-test its own functions as well as to test the other cores within the chip boundary. In BIST methodology, pseudo-random pattern

testing can reduce the memory requirements. In addition to general pseudo-random pattern testing, this paper proposes and evaluates a novel selective-random ...

Keywords: SOC testing, built-in self-test, design for testability, processor-based testing, pseudo-random number generator

16 Test synthesis for mixed-signal SOC paths

Sule Ozev, Ismet Bayraktaroglu, Alex Orailoğlu

January 2000 **Proceedings of the conference on Design, automation and test in Europe DATE '00**

Publisher: ACM Press

Full text available: pdf(98.68 KB) Publisher Site

Additional Information: full citation, references, index terms

17 A hierarchical model of data locality

Chengliang Zhang, Chen Ding, Mitsunori Ogihara, Yutao Zhong, Youfeng Wu

January 2006 **ACM SIGPLAN Notices , Conference record of the 33rd ACM SIGPLAN-SIGACT symposium on Principles of programming languages POPL '06,** Volume 41 Issue 1

Publisher: ACM Press

Full text available: pdf(256.26 KB) Additional Information: full citation, abstract, references, index terms

In POPL 2002, Petrank and Rawitz showed a universal result---finding optimal data placement is not only NP-hard but also impossible to approximate within a constant factor if $P \neq NP$. Here we study a recently published concept called *reference affinity*, which characterizes a group of data that are always accessed together in computation. On the theoretical side, we give the complexity for finding reference affinity in program traces, using a novel reduction that convert ...

Keywords: N-body simulation, NP-complete, hierarchical data placement, program locality, reference affinity, volume distance

18 Real-time shading

Marc Olano, Kurt Akeley, John C. Hart, Wolfgang Heidrich, Michael McCool, Jason L. Mitchell, Randi Rost

August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

Publisher: ACM Press

Full text available: pdf(7.39 MB) Additional Information: full citation, abstract

Real-time procedural shading was once seen as a distant dream. When the first version of this course was offered four years ago, real-time shading was possible, but only with one-of-a-kind hardware or by combining the effects of tens to hundreds of rendering passes. Today, almost every new computer comes with graphics hardware capable of interactively executing shaders of thousands to tens of thousands of instructions. This course has been redesigned to address today's real-time shading capabili ...

19 Compiler construction: an advanced course

F. L. Bauer, F. L. De Remer, M. Griffiths, U. Hill, J. J. Horning, C. H. A. Koster, W. M. McKeeman, P. C. Poole, W. M. Waite, G. Goos, J. Hartmanis

January 1974 Book

Publisher: Springer-Verlag New York, Inc.

Full text available: pdf(65.62 MB) Additional Information: full citation, abstract, references, cited by

The Advanced Course took place from March 4 to 15, 1974 and was organized by the Mathematical Institute of the Technical University of Munich and the Leibniz Computing Center of the Bavarian Academy of Sciences, in co-operation with the European Communities, sponsored by the Ministry for Research and Technology of the Federal Republic of Germany and by the European Research Office, London.

20 Frontmatter (TOC, Letter from the chair, Letter from the editor, Letters to the editor, ACM policy and procedures on plagiarism, PASTE abstracts, Calendar of future events, Workshop and conference information)

ACM SIGSOFT Software Engineering Notes staff

January 2006 **ACM SIGSOFT Software Engineering Notes**, Volume 31 Issue 1

Publisher: ACM Press

Full text available: pdf(1.82 MB) Additional Information: full citation, index terms

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☐	L3	chen.in. and simulation and (test with path?)	9
☐	L2	L1 and intellectual property	4
☐	L1	chen.in. and reuse and simulation	63

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